REMARKS

In response to the Office Action mailed May 12, 2009, Applicants respectfully request reconsideration. Claims 1-15, 17-43, 46-56, and 58-61 were previously pending in this application. Claims 15, 30, 43, 60 and 61 have been amended herein. As a result, claims 1-15, 17-43, 46-56, and 58-61 remain pending for examination with claims 1, 15, 30 and 43 being independent. No new matter has been added.

Allowable Subject Matter

Applicants note with appreciation the indication that claims 1-14 have been allowed, and that claims 34-42 would be allowable if rewritten in independent form.

Summary of Examiner Interview

Applicants' representative appreciates the courtesies extended by Examiner Warren in granting a telephone interview on September 10, 2009. The substance of the interview is summarized herein.

Applicants' representative proposed amending independent claims 15, 30 and 43 to recite a "gate region that extends substantially through an entire thickness of the semiconductor chip" to place the claims in condition for allowance. The Examiner agreed that the proposed amendments appear to distinguish over the art of record. These amendments have been submitted herein. Accordingly, the claims as presented are believed to be in condition for allowance.

Rejections under 35 U.S.C. §112

The Office Action rejected claims 60 and 61 under 35 U.S.C. §112 because claims 60 and 61 recite the limitation "the first region" and "the second region," which lack antecedent basis. In response, claims 60 and 61 have been amended to refer to the source region, the drain region and an intermediary region. Accordingly, withdrawal of the rejection of claims 60 and 61 under 35 U.S.C. §112 is respectfully requested.

Rejections Under 35 U.S.C. §102

I. The Office Action rejected claims 15, 17, 18, 28 and 29 (including independent claim 15) under 35 U.S.C. §102(b) as purportedly being anticipated by Harari (US 4,933,739). Applicants respectfully request reconsideration.

Harari describes trench resistor structures for compact semiconductor memory and logic devices. FIG. 8 of Harari shows a vertical low resistivity connection to a buried collector layer (col. 10, lines 57-60, FIG. 8).

By contrast, claim 15, as amended, recites a MOS-type power component comprising a gate region that extends substantially through an entire thickness of the substrate. Harari does not teach or suggest a gate region that extends substantially through an entire thickness of the substrate. Rather, Harari describes a low resistivity connection to a buried collector layer. For at least this reason, claim 15 patentably distinguishes over Harari. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 17-29 depend from claim 15 and patentably distinguish over Harari for at least the same reasons.

II. The Office Action rejected claims 30-33 (including independent claim 30) under 35 U.S.C. §102(b) as purportedly being anticipated by Gaul et al. (US 6,114,768). Applicants respectfully request reconsideration.

FIG. 7 of Gaul shows a semiconductor device and a via 32 that extends through the P-type substrate 10. As shown in FIG. 7 of Gaul, the gate of the semiconductor device is formed above the surface of the substrate 10.

By contrast, claim 30, as amended, recites a MOS-type power component comprising a gate region that extends substantially through an entire thickness of the semiconductor chip. Gaul does not teach or suggest a gate region that extends substantially through an entire thickness of the semiconductor chip. Rather, as discussed above, the gate of Gaul's device is formed above the surface of the substrate. For at least this reason, claim 30 patentably distinguishes over Gaul. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 31-42 depend from claim 30 and patentably distinguish over Gaul for at least the same reasons.

III. The Office Action rejected claims 15, 17-29, 43, 46-56, 58, and 59 (including independent claims 15 and 43) under 35 U.S.C. §102(a) as purportedly being anticipated by Tihanyi et al. (US 6,459,142). Applicants respectfully request reconsideration.

FIG. 4 of Tihanyi shows a power MOSFET in which the gate electrodes 7 are disposed in trenches 16 filled with insulating material 17. These trenches extend down to the p⁻-conductance layer 18.

By contrast, claim 15, as amended, recites a MOS-type power component comprising a gate region that extends substantially through an entire thickness of the substrate. Tihanyi does not teach or suggest a gate region that extends substantially through an entire thickness of the substrate. Rather, Tihanyi's gate electrode 7 only extends down to the p⁻-conductance layer 18. For at least this reason, claim 15 patentably distinguishes over Tihanyi. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 17-29 depend from claim 15 and patentably distinguish over Tihanyi for at least the same reasons.

Claim 43, as amended, recites a MOS-type power component, comprising a gate region that extends substantially through an entire thickness of the substrate. As should be appreciated from the above discussion, Tihanyi does not teach or suggest a gate region that extends substantially through an entire thickness of the substrate. Therefore, claim 43 patentably distinguishes over Tihanyi. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 46-59 depend from claim 43 and patentably distinguish over Tihanyi for at least the same reasons.

CONCLUSION

In view of the above amendment, Applicants believe the pending application is in condition for allowance. A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, the Director is hereby authorized to charge any deficiency or credit any overpayment in the fees filed, asserted to be filed, or which should have been filed herewith to our Deposit Account No. 23/2825, under Docket No. S1022.81119US00 from which the undersigned is authorized to draw.

Dated: September 22, 2009

Respectfully submitted,

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